How Computers Calculate Square Root?

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Demystifying mathematical-function black box
FLOATING-POINT UNIT DESIGN
USING TAYLOR-SERIES EXPANSION ALGORITHMS

by

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Thesis Proposal

UNIVERSITY OF SOUTHERN CALIFORNIA
ELECTRICAL ENGINEERING

September 2006
How Time Consuming Is SQRT()?

<table>
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<tr>
<th>Design</th>
<th>Cycle time (ns)</th>
<th>Latency/Throughput (cycles/cycles)</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>$a \pm b$</td>
</tr>
<tr>
<td>DEC 21164 Alpha AXP</td>
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<td>4/1</td>
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<td>Intel Pentium</td>
<td>5.0</td>
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<tr>
<td>Intel Pentium Pro</td>
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<td>Sun UltraSparc</td>
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<td>3/1</td>
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</table>

- **Latency**: How many clock cycles to compete 1 operation
- **Throughput**: Cycles before the next operation can be issued
Hardware Implementation of SQRT()

- **Newton-Raphson method**

- **Series expansion**

\[
\sqrt{b} \approx Y_0 \left\{ 1 - \frac{1}{2} \left(1 - \frac{b}{Y_0^2}\right) - \frac{1}{8} \left(1 - \frac{b}{Y_0^2}\right)^2 - \frac{1}{16} \left(1 - \frac{b}{Y_0^2}\right)^3 - \frac{15}{128} \left(1 - \frac{b}{Y_0^2}\right)^4 \right\}
\]

Figure 2.1 Newton-Raphson algorithm for finding the root of \(f(x)\)
Simple SQRT() Routine

• Initial Guess

\[ r = \frac{1}{s^2} \]

\[ \approx f(s) = c_0 + c_1 s + c_2 s^2 + c_3 s^3 \]

\[ = c_0 + s \times ( c_1 + s \times ( c_2 + s \times c_3 ) ) \]

where 0.1 < \( r^2 \) < 1.0

\[ c_0 = 0.188030699; \ c_1 = 1.48359853 \]

\[ c_2 = -1.0979059; \ c_3 = 0.430357353 \]

• Newton-Raphson Refinement

\[ \delta s \leftarrow s - f(s)^2 \]

\[ r \leftarrow f(s) + \delta s / 2f(s) \]

SIMD/Vector Operation

- Each FMA operation can work on a set of multiple operands concurrently
- Single-instruction multiple-data (SIMD) parallelism: An arithmetic operation is operated on multiple operand-pairs stored in vector registers, each of which can hold multiple double-precision numbers.

Example: Vector multiplier (VMUL) loads data from two vector registers, R1 and R2, each holding 4 double-precision numbers, concurrently performs 4 multiplications, and stores the results on vector register R3.