Intel Xeon Phi Programming

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Goal: Multithreading on Intel Xeon Phi
Two Supercomputing Parties in the US

**Titan:** Oak Ridge Nat’l Lab
- 17.6 Petaflop/s
- AMD Opteron + NVIDIA K20x

**Aurora:** Argonne Nat’l Lab (2019)
- 180-450 Petaflop/s
- Intel Xeon Phi

**GPU vs. Phi**
Intel Xeon Phi Processors

Current Knights Landing (KNL) is a predecessor of the Knights Hill (KNH) processor in Aurora
Knights Landing (KNL)

**Knights Landing Overview**

*Chip: 36 Tiles interconnected by 2D Mesh*
*Tile: 2 Cores + 2 VPU/core + 1 MB L2*

*Memory: MCDRAM: 16 GB on-package; High BW*
*DDR4: 6 channels @ 2400 up to 384GB*

*IO: 36 lanes PCIe Gen3. 4 lanes of DMI for chipset*
*Node: 1-Socket only*
*Fabric: Omni-Path on-package (not shown)*

*Vector Peak Perf: 3+TF DP and 6+TF SP Flops*
*Scalar Perf: ~3x over Knights Corner*
*Streams Triad (GB/s): MCDRAM: 400+; DDR: 90+*

VPU: Vector processing unit
MCDRAM: Multi-channel dynamic random access memory (4× bandwidth of DRAM)
• Standard MPI+OpenMP programming is supported
• Should utilize fast on-chip MCDRAM (multi-channel dynamic random access memory) shared by 72 cores
• Should take advantage of AVX-512 (512-bit or 8 double-precision) SIMD operations on vector processing units (VPUs)