Teraflops
Research Chip
Moore’s Law Motivates Multi-Core

More, better transistors
More cores
Continued benefits from Moore’s Law

MICROPROCESSOR TRANSISTOR COUNT

45nm


10^3 10^5 10^7 10^9
What is Tera-scale?

Teraflops of performance operating on Terabytes of data

Performance

TIPS

GIPS

MIPS

KIPS

Dataset Size

Kilobytes

Megabytes

Gigabytes

Terabytes

Tera-scale

3D & Video

Multimedia

Text

Single-core

Multi-core

RMS

Learning & Travel

Entertainment

Personal Media Creation and Management

Health

RMS

Text

Multimedia

Single-core

Multi-core

3D & Video
Intel Tera-scale Research

100+ Research Projects Worldwide

**Microprocessor**
- Examples:
  - Scalable memory
  - **Multi-core architectures**
  - Specialized cores
  - **Scalable fabrics**
  - Energy efficient circuits

**Platform**
- Examples:
  - **3D Stacked Memory**
  - Cache Hierarchy
  - Virtualization/Partitioning
  - Scaleable OS’s
  - I/O & Networking

**Programming**
- Examples:
  - Speculative Multithreading
  - Transactional memory
  - Workload analysis
  - Compilers & Libraries
  - Tools

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ACCELERATE TRANSITION TO PARALLEL PROGRAMMING

University Outreach
Intel® Press
Intel® Software College

www.intel.com/software/products
A Historical Perspective: ASCI Red

1996: First Teraflops Supercomputer Developed by Intel for Sandia National Lab
- 104 cabinets, over 2500sq feet
- Almost 10,000 Pentium® Pro processors
- Consumed 500kw

Source: Intel, 1996
Teraflops Research Chip
100 Million Transistors • 80 Tiles • 275mm²

First tera-scale programmable silicon:
- Teraflops performance
- Tile design approach
- On-die mesh network
- Novel clocking
- Power-aware capability
- Supports 3D-memory

Not designed for IA or product
Tiled Design & Mesh Network

Repeated Tile Method:
- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle

Mesh Interconnect:
- “Network-on-a-Chip”
  - Cores networked in a grid allows for super high bandwidth communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)
- Future: connect IA/or and special purpose cores

* When operating at a nominal speed of 4GHz
Fine Grain Power Management

- Novel, modular clocking scheme saves power over global clock
- New instructions to make any core sleep or wake as apps demand
- Chip Voltage & freq. control (0.7-1.3V, 0-5.8GHz)

Dynamic sleep

STANDBY:
- Memory retains data
- 50% less power/tile

FULL SLEEP:
- Memories fully off
- 80% less power/tile

Industry leading energy-efficiency of 16 Gigaflops/Watt
## Research Data Summary

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Voltage</th>
<th>Power</th>
<th>Bisection Bandwidth</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.16 GHz</td>
<td>0.95 V</td>
<td>62W</td>
<td>1.62 Terabits/s</td>
<td>1.01 Teraflops</td>
</tr>
<tr>
<td>5.1 GHz</td>
<td>1.2 V</td>
<td>175W</td>
<td>2.61 Terabits/s</td>
<td>1.63 Teraflops</td>
</tr>
<tr>
<td>5.7 GHz</td>
<td>1.35 V</td>
<td>265W</td>
<td>2.92 Terabits/s</td>
<td>1.81 Teraflops</td>
</tr>
</tbody>
</table>

**1.01 Teraflops**

**62 Watts**
## Application Performance

At 1.07V, 4.27GHz operation:

<table>
<thead>
<tr>
<th>Application Kernels</th>
<th>FLOP count</th>
<th>Teraflops @ 4.27GHz</th>
<th>% Peak Teraflops</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stencil – PDE Solver</td>
<td>358K</td>
<td>1.00</td>
<td>73.3%</td>
</tr>
<tr>
<td>SGEMM: Matrix Multiplication</td>
<td>2.63M</td>
<td>0.51</td>
<td>37.5%</td>
</tr>
<tr>
<td>Spreadsheet</td>
<td>62.4K</td>
<td>0.45</td>
<td>33.2%</td>
</tr>
<tr>
<td>2D FFT</td>
<td>196K</td>
<td>0.02</td>
<td>2.73%</td>
</tr>
</tbody>
</table>
What’s Next?

- Many Floating-Point Cores
- + Stacked Memory
- Many general-purpose cores
- Next research challenge

Continuously enable new tech 5-10 years out

Research Labs
Product Groups

New Product Development & Design

Future tera-scale processors